We Claim:

1. A sigma-delta programming device, comprising:

an input being configured to receive a digital signal with a word length of N bits, most significant L bits of a data word representing places before a decimal point in a binary number represented by the data word, and remaining N-L less significant bits representing places after the decimal point in the binary number;

a sigma-delta modulator being configured to receive N-L+1 less significant bits of the N-bit data word;

an adder having a first adder input configured to receive L-1 most significant bits of the N-bit data word, a second adder input being configured to receive a signal processed by said sigma-delta modulator, and an output; and

a multiplier configured to multiply a signal from said output of said adder by two.

2. The sigma-delta programming device according to claim 1, wherein said adder adds the L-1 most significant bits of the N-bit data word to the signal processed by said sigma-delta modulator to produce a sum and outputs the sum at said output.

3. The sigma-delta programming device according to claim 1, wherein said sigma-delta modulator is constructed exclusively from single-bit decision makers.

4. A configuration, comprising:

a sigma-delta programming device according to claim 1; and

a programmable frequency divider actuated by said sigma-delta programming device.

5. A PLL frequency synthesizer, comprising:

a sigma-delta programming device according to claim 1; and

a PLL circuit having:

a voltage-controlled oscillator having an output configured to output a modulated output signal,

a phase detector configured to ascertain a phase difference by subtracting a reference signal from a feedback signal derived from the output signal and to actuate said voltage-controlled oscillator based on the ascertained phase difference, and

a feedback loop providing the feedback signal and including a programmable frequency divider controlled by said sigma-delta programming device.

6. The PLL frequency synthesizer according to claim 5, wherein the modulated output signal is a phase-modulated output signal.

7. The PLL frequency synthesizer according to claim 5, wherein the modulated output signal is a frequency-modulated output signal.

8. The PLL frequency synthesizer according to claim 5, further comprising a D/A converter configured to receive the digital signal and having an output connected to a point in said PLL circuit having a high-pass transfer response into said PLL circuit.

9. A method for programming a programmable device using a sigma-delta programming device, which comprises the steps:

inputting a digital signal having a word length of N bits into the sigma-delta programming device, most significant L bits of a data word in the digital signal representing places before a decimal point in a binary number represented by the data word,

and remaining N-L less significant bits representing places after the decimal point in the binary number;

subjecting N-L+1 less significant bits of the N-bit data word to sigma-delta modulation to yield a sigma-delta modulated signal;

adding the L-1 most significant bits of the N-bit data word to a data word in the sigma-delta modulated signal;

multiplying the data word obtained from the addition by two to yield a further data word; and

programming the programmable device using the further data word obtained from the multiplication.

10. The method according to claim 9, wherein the programmable device is a frequency divider.